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Paper – CC 12

unit – 5, Topic – Master slave JK flipflop

MASTER SLAVE J-K FLIP-FLOP

In some clocked J-K flip-flop, there may still be some ambiguity in the output when J=K=1 input is applied. This arises due to a race around condition in which the change in state of signals Q, $\bar{Q}$ fedback from output to input of AND gates on applying CP, may cause an oscillatory condition for the duration of the clock pulse (CP). Therefore when CP ends, outputs may be quite arbitrary, depending upon the propagation delay through the flip-flop and the duration of CP.

A circuit to avoid this race around condition is called a J-K master slave flip-flop. Its simplified diagram is shown in fig 1, while a bit descriptive in fig 2.

As is obvious from the fig2, at the input of the slave, trigger (CP) appear after inversion. As T=1, $\bar{T}$ will be 0. Therefore slave R-S flip flop cannot change its state (inhibited) and Q_n is invariant for pulse duration. This is the situation when master is enabled. But when trigger pulse passes, T=0 so that master is inhibited and as $\bar{T}$ =1, slave will be enabled. Since slave is a R-S flip-flop, its operation follows R-S flip-flop truth table.

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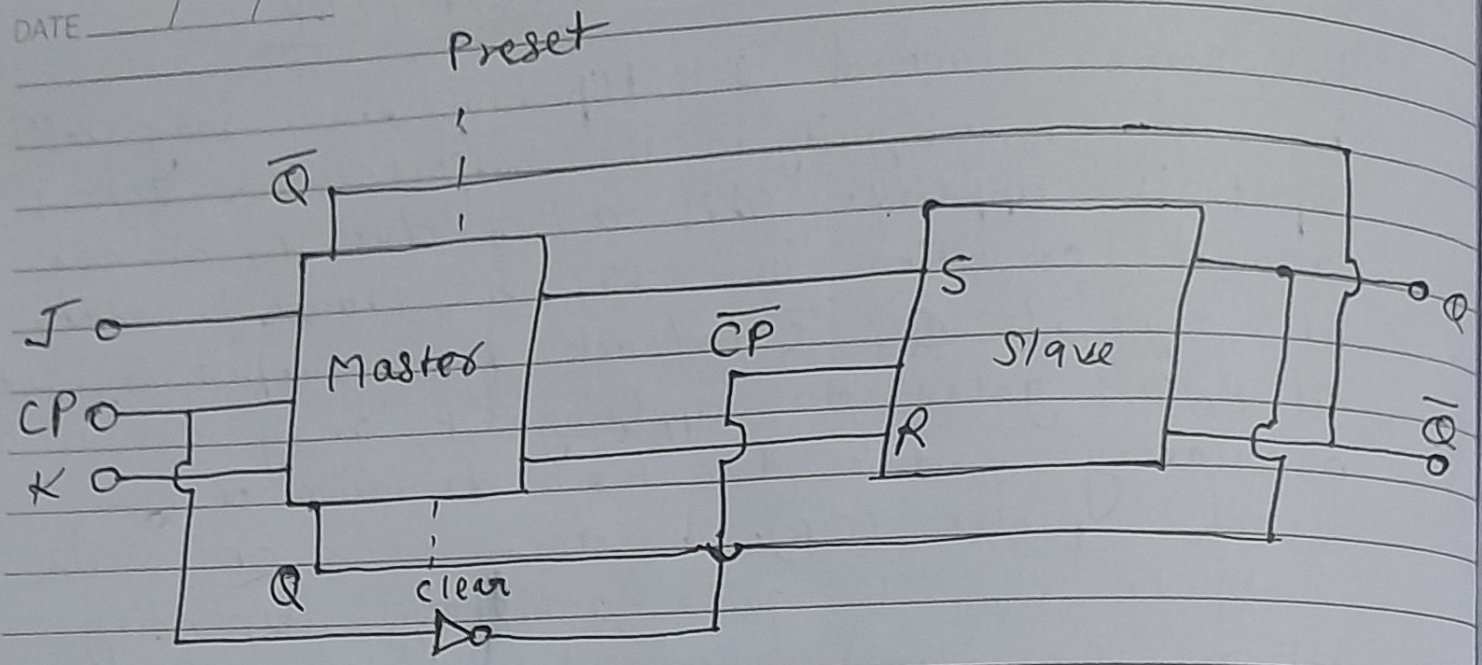

fig 1. Simplified block diagram of J-K master slave flip-flop

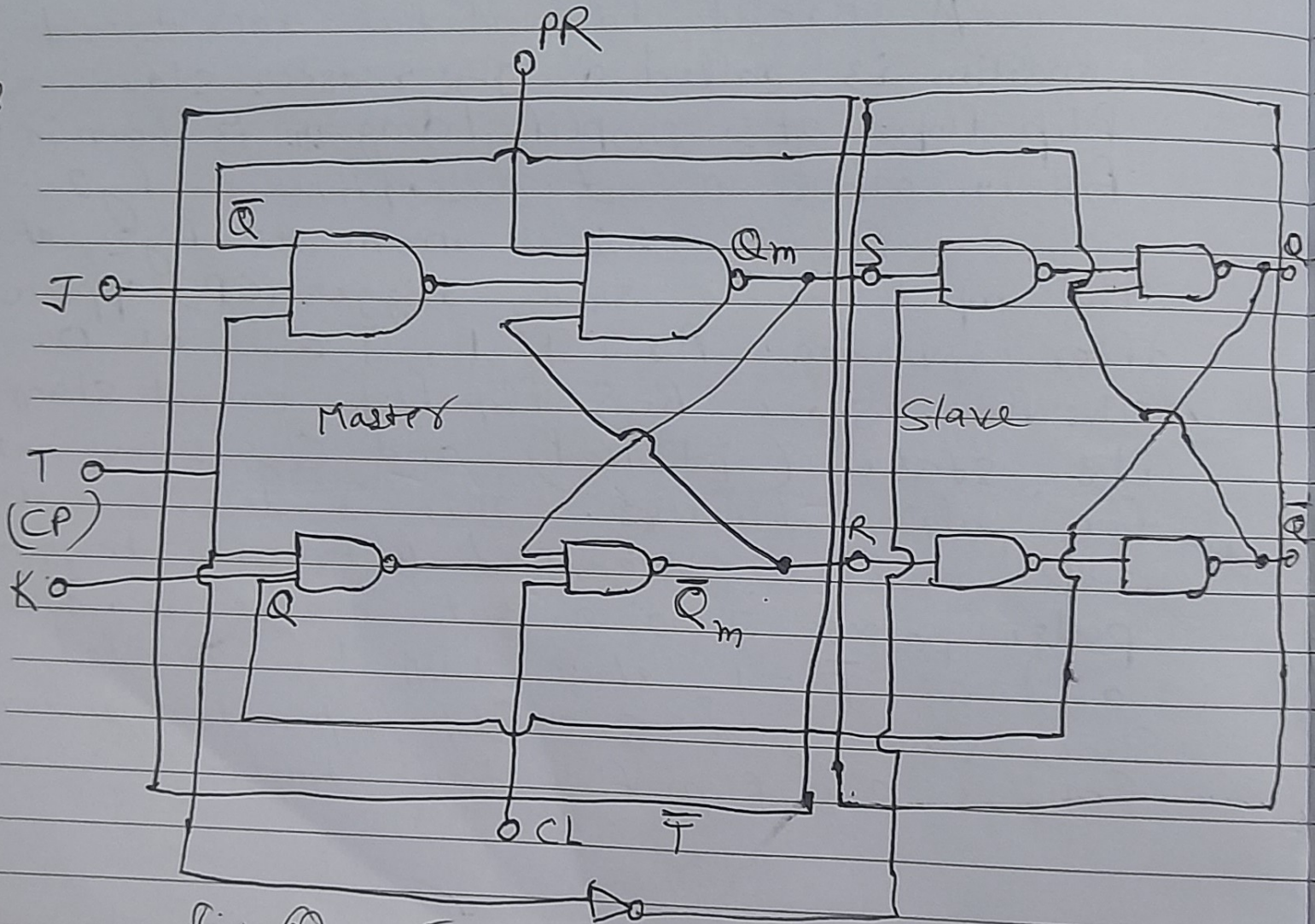

fig ② J-K Master Slave flip-flop

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If $S = Q_m = 1$ and $R = \bar{Q}_m = 0$
then $Q = 1$ and $\bar{Q} = 0$

If $S = Q_m = 0$ and $R = \bar{Q}_m = 1$
then $Q = 0$ and $\bar{Q} = 1$

Thus in the interval between clock pulses, the value of Q_m is transferred to the output Q (or $\bar{Q}_m$ is transferred as $\bar{Q}$). Erratic behaviour does not occur during the block pulse, because the cross connected feedback is from the output of the slave to the input of the master. Since the outputs Q and $\bar{Q}$ do not change during the clock pulse, no oscillations can take place. Thus possibility of arbitrary outputs when CP ends are removed.